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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/000,158	Applicant(s) KHANNA ET AL.	
	Examiner Hashem Farrokh	Art Unit 2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-4,6-7,9-15,17-19,21-30,32-43,45-47,49-51,53-54,56-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-4,7,11-15,17,21,24-29,33,34,37,39-43,45-47,49-51,54 and 56-60* is/are rejected.

7)☐ Claim(s) *6,9,10,18,19,22,23,30,32,35,36,38 and 53* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4,6,9* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

The instant application having application No. 10/000158 has a total of 51 claims pending in the application; there are 8 independent claims and 43 dependent claims, all of which are ready for examination by the examiner.

INFORMATION CONCERNONG CLAIMS

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2-4, 7,11-15, 17,21, 24-28, 39-43, 45-47, 49-51, and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over to Lattibeaudiere (U.S. Patent No. 5436535) in view of Abbott (U.S. Patent No. 6,351,142 B1).

1. In regard to claim 1, Lattibeaudiere teaches: "a method of operating a content addressable memory (CAM) device, comprising:" **(e.g., see column 4 lines 15-20)** "comparing the comparand with data stored in a CAM array" **(e.g., see column 17 lines 67-68, column 18 lines 1-6).** Comparand or search/key data is the input data to be compared/matched with the stored data in the CAM. This data is often stored in a Comparand or search/key register at the input of a CAM device.

"receiving an input data having a plurality of bit group," **(e.g., see column 3 lines 32-40, Figures 2a-2c)** "wherein a first bit group has a first position in the input data relative

to the other bit group," **(e.g., see paragraph 3 lines 32-40, paragraph 5 lines 60-66, and Figures. 2a-2c).** For example DATA_WRITE_CMD field (bits 24-31) in Figure2a. "wherein the input data has a second bit group having second position in the input data relative to the other bit group;" **(e.g., see paragraph 4 lines 20-26, paragraph 5 lines 60-66, and Figures. 2a-2c).** For example CAM_ADDR field in Figure2a. However, Lattibeaudiere does not teach: "translating, in response to first translation information, the first bit group from the first position to a different position in a comparand; translating the second bit group from the second position to second position of the comparand in response to second translation information; selecting the first translation information in a first cycle and the second translation information in a second cycle;"

Abbott shows a field programmable logic data path that may be used in a field programmable device to perform various logic functions **(e.g., see the abstract).** As an example, he shows that programmable logic data path may be configured to perform the CAM operation **(e.g., see column 17 lines 11-14 and also the claims, columns 20-24).**

Referring to claim 1, Abbott teaches: "translating, in response to first translation information, the first bit group from the first position to a different position in a comparand;" **(e.g. see column 7 lines 1-15, Figure 3A and 3B).** "translating, the second bit group from the second position to second position of the comparand in response to second translation information;" **(e.g., see column 6 lines 65-67).** Although, a 3-bit field, in a 48-bit array, has been shown as an example, the reference teaches that that rearrangement circuit 202 can be adapted for various rearrangement

of any bit field widths **(column 7 lines 26-30)** and relative bit position **(column 6 line 67).** It is understood by those skilled in art that rearrangement circuits along with control circuitry shown in Figure2 perform the translation function indicated in the instant application. "selecting the first translation information in a first cycle and the second translation information in a second cycle;" **(e.g., see abstract, also column 6 lines 48-51).**

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine in the Contend Addressable Memory system of Lattibeaudiere with the circuits taught by Abbott. The modification would have provided dynamic programmability in performing a number of logical operations **(e.g., see abstract).** It is understood by those skilled in art that Programmable Logics Devices (PLDs) are often used to implement various circuit functions during design and proto typing. The programmability feature of these devices, gives the designer the flexibility to test and verify their design before committing to manufacturing, which in turn reduces the cost and time involved with repeated manufacturing processes.

2. In regard to claim 2, Abbott teaches: "The method of claim 1, further comprising decoding the first translation information" **(e.g. see column 7 lines 12-13 and element 112 in Figure2).**

3. In regard to claim 3, Lattibeaudiere teaches: "The method of claim 2, further comprising programming the CAM device with the first translation information" **(e.g., see column 4 lines 15-21).**

4. In regard to claim 4, Abbott teaches: "The method of claim 2, wherein translating comprises establishing switch connection between the first position of the input data and the position of comparand" **(e.g. see column 7 lines 1-15, Figures 3A and 3B)**. The output of the rearrangement circuitry is the CAM comparand.

5. In regard to claim 7, Abbott teaches: "The method of claim 1, further comprising sequentially translating the first and second bit group into the comparand." **(e.g., see abstract and column 6 lines 48-51).**

6. In regard to claim 11, Abbott teaches: "The method of claim 3, wherein the first translation information determines the position of the comparand register that the first bit group is translated to" **(e.g., see column 7 lines 1-15 and Figure 3A).** The input bits (bit-groups or field) can be selectively routed to output. The rearrangement circuitry can be used to rearrange the positions of the bits (bit-groups or fields) at the outputs. The corresponding control bits (translation information), which make the rearrangement (translation) are uniquely identifiable.

7. In regard to claim 12, Abbott teaches: "The method of claim 3, wherein the first translation information determines which bit group of plurality of bit groups is to be the first bit group translated to different position in comparand" **(e.g., see column 7 lines 1-15 and Figure 3A).**

8. In regard to claim 12, Abbott teaches: "The method of claim 1, wherein receiving comprises receiving the input from a processor" **(e.g., see column 19 lines 33-38).** The field programmable device (which rearrangement circuitry is part of) can be configured to operate under control of processor (CPU).

9. In regard to claim 14, Lattibeaudiere teaches: "An apparatus, comprising: a content addressable memory (CAM) array to receive a comparand" **(e.g., see column 17 lines 66-68 and column 18 lines 1-3)** "the output coupled to the CAM array to transmit the comparand to the CAM array" **(e.g., see column 17 lines 66-68),** but does not teach: **"**a translation circuitry having at least one first input, at least one second input, and at least one output, wherein the first input is configured to receive an input data having the plurality of bit groups, wherein a first bit group has a first position in the input data relative to other bit groups, wherein the second input is configured to receive the translation information indicative of translation of the first bit group from the first position to a different position in a comparand; and wherein the translation information comprises: a switch circuit; a storage element to store the translation information; and a decode circuitry coupled to the storage element to decode the translation information and to establish a connection in the switch circuit between the first position and position in comparand."

Abbott teaches "a translation circuitry having at least one first input," **(e.g., see column 7 line 5 and Figure2)** "at least one second input," **(e.g., see column 7 lines 13-15 and output from element 112 in Figure2)** "and at least one output," **(e.g., see column 7 line 5)** "wherein the first input is configured to receive an input data having the plurality of bit groups," **(e.g., see column 7 lines 5)** "wherein a first bit group has a first position in the input data relative to other bit groups," **(e.g., see column 7 lines 1-15 and Figure 3A)** "wherein the second input is configured to receive the translation information indicative of translation of the first bit group from the first position to a

different position in a comparand;" **(e.g. see column 7 lines 1-15, Figure 3A and 3B, and elements 112 and 202 in Figure2).** "and wherein the translation circuitry comprises: a switch circuit;" **(e.g., see column 7 lines 1-15, Figure 3B)** "a storage element to store the translation information;" **(e.g.; see column 5 lines 28-31 and 41-42)** "and a decode circuitry coupled to the storage element to decode the translation information and establish a connection in the switch circuit between the first position and position in comparand." **(e.g., see column 5 lines 24-39, elements 110 and 112 in Figure1, and Figures 3A-3B).**

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the system of Lattibeaudiere with the circuits taught by Abbott. The modification would have provided dynamic programmability in performing a number of logical operations (e.g., see abstract). It is understood by those skilled in art that Programmable Logics Devices are often used to implement various circuit functions during the design and proto typing. The programmability feature of these devices, gives the designer the flexibility to test and verify their design before committing to manufacturing, which in turn reduces the cost and time involved with repeated manufacturing processes.

10. In regard to claim 15, Lattibeaudiere teaches: "The apparatus of claim 14, further comprising a comparand storage element coupled between the CAM array and translation circuitry to store the comparand" **(e.g., see column 17 lines 66-68, column 18 line 1-3).**

11. In regard to claim 17, Abbott teaches: "The apparatus of claim 6, wherein the switch circuit comprises at least one multiplier." **(e.g., see column 7 line 7, Figure 3B).**

12. In regard to claim 21, Abbott teaches: "The apparatus of claim 14, further comprising an input bus coupled to the first input of the translation circuit and wherein the switch circuit comprises a plurality of multiplexes each coupled to the input bus." **(e.g., see column 6 lines 58-62, Figure 3B).**

13. In regard to claim 24, Lattibeaudiere teaches: "The apparatus of claim 14, wherein the apparatus further comprises: a plurality of storage element, each of the plurality of storage element to store a portion of translation information;" **(e.g., column 9 lines 26-36 and Figure 5)** "selection circuitry coupled to plurality of storage element to select from the plurality of storage elements;" **(e.g., see column 11 lines 2-39, elements U6 and U8 in Figure 5).** The combination of ROM and address counter generates addresses for EPROM, which provides the control signals for the CAM system including select signals (see Figure6). Lattibeaudiere, however, does not teach "and a decode circuit coupled to the plurality of selection circuitry to decode the portion of the translation information and to establish a switch circuit connection between the first position and the position in the comparand"

Abbott teaches: teach "a decode circuit coupled to the plurality of selection circuitry to decode the portion of the translation information and to establish a switch circuit connection between the first position and the position in the comparand." **(e.g., see column 7 lines 1-15 and elements 108 and 112 in Figure1 and Figure 3A).**

14. In regard to claim 25, Lattibeaudiere teaches: "The apparatus of claim 24, wherein each of the plurality of storage elements to store a portion of translation information for one cycle of plurality of cycles, and the selection circuitry to select from among the plurality of storage elements based on a particular cycle of plurality of cycles" **(e.g., see column 11 lines 40-52 and Figure 5).** The combination of ROM and address counter generates addresses to access the translation information stored in the EPROM.

15. In regard to claim 26, Lattibeaudiere teaches: "The apparatus of claim 25, further comprising a comparand register coupled between the CAM array and the translation circuitry to store the comparand" **(e.g., see column 17 lines 67-68).**

16. In regard to claim 27, Abbott teaches: "The method of claim 26, further comprising a processor coupled to the first input of the translation circuitry to transmit the input data" **(e.g., see column 19 lines 33-38, Figure 1).** The field programmable device (which rearrangement circuitry is part of) can be configured to operate under control of a processor (CPU).

17. In regard to claim 28, Abbott teaches: "The method of claim 14, further comprising a processor coupled to the first input of the translation circuitry to transmit the input data" **(e.g., see column 19 lines 33-38, Figure 1).** The field programmable device (which rearrangement circuitry is part of) can be configured to operate under control of a processor (CPU).

18. In regard to claim 39 Lattibeaudiere teaches: "A content addressable memory (CAM) device, comprising: a CAM array to receive a comparand;" **(e.g., see column 17**

lines 67-68, column 18 lines 1-3) "the output coupled to CAM array to transmit the comparand to the CAM array; " **(e.g., see column 4 lines 15-21 and elements 62 and 70 in Figure 6),** but does not teach "a switch circuit having an input and an output, the input configured to receive input data having a plurality of bit groups, wherein a first bit group has a first position in the input data relative to other bit groups; a storage element to store a translation information indicative of a translation of the first bit group from the first position to different position in the comparand.

Abbott, however teaches: "a switch circuit having an input and an output, the input configured to receive input data having a plurality of bit groups, wherein a first bit group has a first position in the input data relative to other bit groups;" **(e.g., see column 7 lines 1-15, element 202 in Figure 2 and Figures 3A-3B)** "a storage element to store a translation information indicative of a translation of the first bit group from the first position to different position in the comparand. " **(e.g., see column 5 lines 24-39 element 110 in Figure1 and Figure 3A).** The control unit 110 contains control vector (bits), which provides information indicative of rearrangement (translation) of bit groups from input to output.

19. In regard to claim 40, Lattibeaudiere teaches: "The CAM device of claim 39, " **(e.g., see abstract)** "further comprising: a decode circuitry coupled to the storage element to decode the translation information and to establish a switch circuit connection in the switch circuit between the first position and position in comparand."

However, Abbott teaches" "further comprising: a decode circuitry coupled to the storage element to decode the translation information and to establish a switch circuit

connection in the switch circuit between the first position and position in comparand." **(e.g., see column 5 lines 24-39,column 7 lines 1-15, elements 110 and 112 in Figure1, and Figure 3A).**

20. In regard to claim 41, Lattibeaudiere teaches: "The CAM device of claim 40, " **(e.g., see abstract)** but does not teach: "further comprising: a plurality of additional storage elements, the storage element and each of the plurality of additional storage elements to store a portion of translation information for one cycle of plurality of cycles; and selection circuitry coupled to the storage element and the plurality of additional storage elements to select from among the storage element and the plurality of additional storage elements based on a particular cycle of plurality of cycles for transmission to decode circuitry"

Abbott teaches: "further comprising: a plurality of additional storage elements, **(e.g., see column 5 lines 28-31)** "the storage element and each of the plurality of additional storage elements to store a portion of translation information for one cycle of plurality of cycles; **(e.g., see column 6 lines 48-51)** "and selection circuitry coupled to the storage element and the plurality of additional storage elements to select from among the storage element and the plurality of additional storage elements based on a particular cycle of plurality of cycles for transmission to decode circuitry" **(e.g., see column 5 lines 24-49 elements 108, 110, and 112 in Figure 1).** The control vector selected from memory (see column 5 lines 39-40) and coupled to the decoder 110. Decoder circuits drive the switching circuits (multiplexers), which make the rearrangement (translation) of input fields (bit-groups).

21. In regard to claim 42, Lattibeaudiere teaches: "The CAM device of claim 41, further comprising a comparand register coupled between the CAM array and the switch to store the comparand" **(e.g., column 17 lines 67-68).**

22. In regard to claim 42, Lattibeaudiere teaches: "An apparatus comprising: a content addressable memory (CAM) array;" **(e.g., see the abstract),** but does not teach "and means for translating, in response to translation information, a bit group from a position of an input data having a plurality of bit groups to a different position in a comparand, wherein the means for translating comprises: means for storing the translation information; and means for decoding the translation information."

Abbott teaches: "and means for translating, in response to translation information, a bit group from a position of an input data having a plurality of bit groups to a different position in a comparand, **(e.g., see column 7 lines 1-15 Figures 3A-3B)** "wherein the means for translating comprises: means for storing the translation information; **(e.g., see column 5 lines 24-42 and element 110 in Figure 1)** "and means for decoding the translation information." **(e.g., see column 7 lines 12-15 element 112 in Figure 1).**

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine in the Contend Addressable Memory system of Lattibeaudiere with the circuits taught by Abbott. The modification would have provided dynamic programmability in performing a number of logical operations **(e.g., see abstract).** It is understood by those skilled in art that Programmable Logics Devices are often used to implement various circuit functions during design and proto typing.

The programmability feature of these devices, gives the designer the flexibility to test and verify their design before committing to manufacturing, which in turn reduces the cost and time involved with repeated manufacturing processes.

23. In regard to claim 45, Abbott teaches: "The apparatus of claim 43 wherein the translating comprises means for selecting the translation information from a plurality of translation information" **(e.g., see column 5 lines 24-31 and lines 39-40).**

24. In regard to claim 46, Lattibeaudiere teaches: "An article comprising a machine readable medium that stores data representing an integrated circuit, **(e.g., see column 1 lines 5-7).** It is understood by those skilled in art that a memory device is fabricated using integrated circuit technology. "comprising: a content addressable memory (CAM) array to receive a comparand" **(e.g., see column 2 lines 19-25)** "the output coupled to the CAM array to transmit the comparand to the CAM array" **(e.g., see column 17 lines 66-68),** but does not teach: **"**a translation circuitry having at least one first input, at least one second input, and at least one output, wherein the first input is configured to receive an input data having the plurality of bit groups, wherein a first bit group has a first position in the input data relative to other bit groups, wherein the second input is configured to receive the translation information indicative of translation of the first bit group from the first position to a different position in a comparand; and wherein the translation information comprises: a switch circuit; a storage element to store the translation information; and a decode circuitry coupled to the storage element to decode the translation information and to establish a connection in the switch circuit between the first position and position in comparand."

Abbott teaches "a translation circuitry having at least one first input," **(e.g., see column 7 line 5 and Figure2)** "at least one second input," **(e.g., see column 7 line 5 and output from element 112 in Figure 2)** "and at least one output," **(e.g., see column 7 lines 5)** "wherein the first input is configured to receive an input data having the plurality of bit groups," **(e.g., see column 7 lines 1-15)** "wherein a first bit group has a first position in the input data relative to other bit groups," **(e.g., see column 7 lines 1-15 and Figure 3A)** "wherein the second input is configured to receive the translation information indicative of translation of the first bit group from the first position to a different position in a comparand;" **(e.g. see column 7 lines 1-15, Figure 3A and 3B, and elements 112 and 202 in Figure2).** "and wherein the translation circuitry comprises: a switch circuit;" **(e.g., see column 7 lines 1-15, Figure 3B)** "a storage element to store the translation information;" **(e.g.; see column 5 lines 28-31)** "and a decode circuitry coupled to the storage element to decode the translation information and establish a connection in the switch circuit between the first position and position in comparand." **(e.g., see column 5 lines 24-39, elements 110 and 112 in Figure 1, and Figures 3A-3B).**

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the system of Lattibeaudiere with the circuits taught by Abbott. The modification would have provided dynamic programmability in performing a number of logical operations (e.g., see abstract). It is understood by those skilled in art that Programmable Logics Devices often used to implement various circuit functions during design and proto typing. The programmability

feature of these devices, gives the designer the flexibility to test and verify their design before committing to manufacturing, which in turn reduces the cost and time involved with repeated manufacturing processes.

25. In regard to claim 47, Abbott teaches: "The article of claim 46, wherein the translation circuitry comprises a switch circuit" **(e.g., see column 7 lines 1-15, Figures 2 and 3B).** Multiplexers are used as switching circuits.

26. In regard to claim 49, Lattibeaudiere teaches: "A content addressable memory (CAM) device, comprising:" **(e.g., see the abstract)**

"means for comparing the comparand with data stored in a CAM array" **(e.g., see column 4 lines 15-20, column 17 lines 67-68)** "means for receiving an input data having a plurality of bit group," **(e.g., see column 3 lines 32-39, Figures 2a-2c)** "wherein a first group has a first position in the input data relative to the other bit group," **(e.g., see paragraph 3 lines 32-40, paragraph 5 lines 60-66, and Figures. 2a-2c)** "wherein the input data has a second bit group having second position in the input data relative to the other bit group;" **(e.g., see paragraph 3 lines 32-40, paragraph 5 lines 60-66, and Figures 2a-2c)**. However, Lattibeaudiere does not teach: "means for translating, in response to first translation information, the first bit group from the first position to a different position in a comparand; means for translating the second bit group from the second position to second position of the comparand in response to second translation information; and means for selecting the first translation information in a first cycle and the second translation information in a second cycle;"

Abbott teaches: "means for translating, in response to first translation information, the first bit group from the first position to a different position in a comparand;" **(e.g. see column 7 lines 1-15, Figures 3A and 3B).** "means for translating, the second bit group from the second position to second position of the comparand in response to second translation information;" **(e.g., see column 6 lines 65-67).** Although, a 3-bit field, in a 48-bit array, has been shown as an example, the reference teaches that that rearrangement circuit 202 can be adapted for various rearrangement of any bit field widths **(column 7 lines 26-30)** and bit position **(column 6 line 67).** It is understood by those skilled in art that rearrangement circuits along with control circuitry shown in Figure2 perform the translation function indicated in the instant application. "means for selecting the first translation information in a first cycle and the second translation information in a second cycle;" **(e.g., see abstract, column 6 lines 48-51).**

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine in the contend addressable memory system of Lattibeaudiere with the circuits taught by Abbott. The modification would have provided dynamic programmability in performing a number of logical operations **(e.g., see abstract).** It is understood by those skilled in art that Programmable Logics Devices are often used to implement various circuit functions during design and proto typing. The programmability feature of these devices, gives the designer the flexibility to test and verify their design before committing to manufacturing, which in turn reduces the cost and time involved with repeated manufacturing processes.

27. In regard to claim 50, Abbott teaches: "The apparatus of claim 49, further comprising means for decoding the first translation information" **(e.g. see column 7 lines 9-15, Figures 3A and 3B).**

28. In regard to claim 51, Lattibeaudiere teaches: "The apparatus of claim 49, further comprising means for programming the CAM device with the first translation information" **(e.g., see column 4 lines 15-20).**

29. In regard to claim 54, Abbott teaches: "The apparatus of claim 49, further comprising means for sequentially translating the first and second bit groups into comparand **(e.g., see the abstract).** The operation chip is performed cycle-by-cycle (sequentially).

Claims 29, 33-34, AND 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over to Miller et al (U.S. Patent Publication No. 20030005146) in view of Abbott (U.S. Patent No. 6,351,142 B1).

30. In regard to claim 29, Miller et al teaches: "An apparatus, comprising: a content addressable memory (CAM) array having a plurality of blocks each configured to receive a comparand; and" **(e.g., see abstract and paragraph 32 in page 7)** but does not teach "a plurality of translation circuitry, each of the plurality of translation circuitry coupled to corresponding one of the plurality of CAM blocks, each translation circuitry having at least one first input, at least one second input, and at least one output, wherein the first input configured to receive an input data having a plurality of bit groups, wherein the first bit group has a first position in the input data relative to the other bit

groups, wherein the second input is configured to receive translation information indicative of translation of the first bit group from the first position to different position in comparand receive by a respective CAM block, the output coupled to the CAM array to transmit the comparand to the CAM block, wherein each of the plurality of translation circuitry is configured to translate the plurality of bit groups over multiple operation cycles"

Abbott however teaches "a plurality of translation circuitry, each of the plurality of translation circuitry coupled to corresponding one of the plurality of CAM blocks, **(e.g., see column 7 lines 6-15 and 26-30).** It should be understood by those skilled in art that while one rearrangement (translation) circuitry shown in the reference, it can be adapted to make as many circuits as is desired by using the same or additional PLDs. "each translation circuitry having at least one first input," **(e.g., see column 7 line 5 and Figure 2)** "at least one second input," **(e.g., see column 7 line 6-15 and output from element 112 in Figure 2)** "and at least one output," **(e.g., see column 7 lines 5)** "wherein the first input is configured to receive an input data having the plurality of bit groups," **(e.g., see column 6 lines 42-46)** "wherein a first bit group has a first position in the input data relative to other bit groups," **(e.g., see column 7 lines 1-15 and Figure 3A)** "wherein the second input is configured to receive the translation information indicative of translation of the first bit group from the first position to a different position in a comparand received by a respective CAM block," **(e.g. see column 7 lines 1-15, Figures 3A and 3B, and elements 112 and 202 in Figure 2)** "the output coupled to transmit the comparand to the CAM block," **(e.g. the output of**

rearrangement circuitry in PLD is connected to the input of each CAM block). "wherein each of the plurality of translation circuitry is configured to translate the plurality of bit groups over multiple operation cycles" **(e.g., see the abstract; it describes the operation is performed in cycle-by cycle basis).**

The PLDs can be configured to perform one or more of a variety of application. Furthermore, the one or more function may be dynamically (e.g, on a cycle-by-cycle basis) programmed into the PLD **(column 17 lines 5-10)**. As an example, the reference implements a CAM function using the PLD. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the CAM blocks of Miller et al to the rearrangement (translation) circuits taught by Abbott. The modification would have provided dynamic programmability in performing a number of logical operations (e.g., see abstract). It is understood by those skilled in art that Programmable Logics Devices are often used to implement various circuit functions during design and proto typing. The programmability feature of these devices, gives the designers the flexibility to test and verify their design before committing to manufacturing, which in turn reduces the cost and time involved with repeated manufacturing processes.

31. In regard to claim 33, Abbott teaches: "The apparatus of claim 29, wherein each of the translation circuitry comprises a switch circuit" **(e.g., see column 7 lines 1-15, Figure 3B).** multiplexers along with decoder are used as switching circuits.

32. In regard to claim 34, Abbott teaches: "The apparatus of claim 33, wherein the switch circuit of at least one of the translation circuitry comprises at least one multiplexer." **(e.g., see column 7 line 7, Figure 3B).**

33. In regard to claim 37, Abbott teaches: "The apparatus of claim 29, wherein the apparatus further comprises: "a plurality of storage element to store the translation information; and" **(e.g., see column 5 lines 28-31 and lines 50-55).** The control vectors (translation information), which control the operation of rearrangement circuit are stored in storage elements. "a decode circuitry coupled to the plurality of selection circuitry to decode the portion of the translation information and to establish a switch circuit connection between the first position and the position in the comparand" **(e.g., see column 6 lines 24-31 and elements 108, 110 in Figure1; column 7 lines 1-15 and Figures 3A-3B)**

Claims 56-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over to Feldmeier (U.S. Patent No. 5920886) in view of Abbott (U.S. Patent No. 6,351,142 B1).

34 In regard to claim 46, Feldmeier teaches: "An apparatus comprising: a content addressable memory (CAM) array to receive a comparand" **(e.g., see paragraph 22 in page 16)** "the output coupled to the CAM array to transmit the comparand to the CAM array," **(e.g., see abstract, paragraph 22 in page 16)** "wherein the translation circuitry comprises a switch having at least one demultiplexer" **(e.g., see paragraph 30 in page 18, element 1620 in Figure16)** but does not teach: "a translation circuitry having at least one first input, at least one second input, and at least one output, wherein the first

input is configured to receive an input data having the plurality of bit groups, wherein a first bit group has a first position in the input data relative to other bit groups, wherein the second input is configured to receive the translation information indicative of translation of the first bit group from the first position to a different position in a comparand;"

Abbott teaches "a translation circuitry having at least one first input," **(e.g., see column 7 line 5 and Figure 2)** "at least one second input," **(e.g., see column 7 line 12-15 and output from element 112 in Figure 2)** "and at least one output," **(e.g., see column 7 line 5)** "wherein the first input is configured to receive an input data having the plurality of bit groups," **(e.g., see column 7 lines 4-7)** "wherein a first bit group has a first position in the input data relative to other bit groups," **(e.g., see column 7 lines 1-15 and Figure 3A)** "wherein the second input is configured to receive the translation information indicative of translation of the first bit group from the first position to a different position in a comparand;" **(e.g. see column 7 lines 1-15, Figures 3A and 3B, and elements 112 and 202 in Figure 2).**

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the system of Feldmeier with the circuits taught by Abbott. The modification would have provided dynamic programmability in performing a number of logical operations (e.g., see abstract). It is understood by those skilled in art that PLDs often used to implement various circuit functions during design and proto typing. The programmability feature of these devices, gives the designer the flexibility to

test and verify their design before committing to manufacturing, which in turn reduces the cost and time involved with repeated manufacturing processes.

35. In regard to claim 57, Abbott teaches: "The apparatus of claim 56, wherein the apparatus further comprises: "a plurality of storage elements, each of the plurality of storage elements to store a portion of the translation information" **(e.g., see column 5 lines 28-31 and lines 50-55).** The control vectors (translation information), which control the operation of rearrangement circuit, are stored in storage elements. "selection circuitry coupled to the plurality of storage elements to select from among the plurality of storage elements; and " **(e.g., see column 5 lines 39-50, elements 104, 106, AND 108 in Figure 1).** The control vectors are selected from plurality of storage element. "A decode circuitry coupled to the plurality of selection circuitry to decode the portion of the translation information and to establish a switch circuit connection between the first position and the position in the comparand" **(e.g., see column 6 lines 24-31 and elements 108, 110 in Figure 1; column 7 lines 1-15 and Figures 3A-3B)**

36. In regard to claim 58, Abbott teaches: "The apparatus of claim 57, wherein each of the plurality of storage elements to store a portion of translation information for one cycle of plurality of cycles, and the selection circuitry to select from among the plurality of storage elements based on a particular cycle of plurality of cycles" **(e.g., see abstract 11).**

37. In regard to claim 59, Miller et al teaches: "The apparatus of claim 58, further comprising a comparand register coupled between the CAM array and the translation

circuitry to store the comparand" **(e.g., see paragraph 22 in page 16, elements 1000 in Figures 10A-10B).**

38. In regard to claim 60, Abbott teaches: "The apparatus of claim 59, further comprising a processor coupled to the first input of the translation circuitry to transmit the input data" **(e.g., see column 19 lines 33-38).** Abbott describes the configuration of the field programmable devices (which rearrangement circuitry is part of) to operate as a co-processing devices under control of processor (CPU). The input connections include connection to the control logic unit and selector unit (elements 110 and 112 in Figure 1).

ALLOWABLE SUBJECT MATTER

1. Claims 6, 9-10, 18-19, 22-23, 30, 32, 35-36, 38, and 53 are objected to as being dependent upon a rejected based claims, but would be allowable if rewritten in and independent form including all of the limitations of the base claim and any intervening claims.

The primary reason for allowance of claims 6, 30, 38, and 53 in instant application is the combination with the inclusion in these claims that the **concurrent translation of bit groups.**

The primary reason for allowance of claims 9-10 and 22-23 in instant application is the combination with the inclusion in these claims that of **bus width among the input data, input bus, and comparand**

Any inquiry of a general nature or relating status of this application or proceeding should be directed to receptionist whose telephone number is (703) 305-3900.

HF

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Donald Sparks

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Supervisory Patent Examiner

Art Unit 2187